QDD-400G-DR4-PRO

Juniper Networks® QDD-400G-DR4 Compatible TAA Compliant 400GBase-DR4 QSFP-DD Transceiver (SMF, 1310nm, 500m, DOM, 0 to 70C, MPO)

Features

- INF-8628 Compliance
- MPO Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free

Applications:

- 400GBase Ethernet
- Access and Enterprise

Product Description

This Juniper Networks® QDD-400G-DR4 compatible QSFP-DD transceiver provides 400GBase-DR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is guaranteed to be 100% compatible with the equivalent Juniper Networks® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Proline's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.

Rev. 030524

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Maximum Power Supply Voltage	V_{CC}	0	3.6	V	1, 2
Storage Temperature	Ts	-40	+85	°C	1, 2
Low-speed Input	Vin	-0.5	Vcc + 0.3	V	1, 2
Recommended Operating Conditions					
Case Operating Temperature	Top	0	+70	°C	
Relative Humidity (non-condensing)	RH	5	85	%	

Notes:

1. Absolute Maximum Ratings are those beyond which damage to the device may occur.
2. Between the Recommended Operating conditions and Absolute Maximum ratings, prolonged operation is not intended, and permanent device degradation may occur.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.10	3.3	3.47	V	
Power Consumption				10	W	1
Low Speed Electrical Interface						
Low Speed Outputs: ModPrsL, IntL	VOL	0		0.4	V	Iol = 2mA
	VOH	Vcc-0.5		Vcc+0.3	V	
Low Speed Inputs: ModSelL, ResetL	VIL	-0.3		0.8	V	
	VIH	2		Vcc+0.3	V	
SCL, SDA Input	VIL	-0.3		Vcc*0.3	V	
	VIH	Vcc*0.7		Vcc+0.5	V	
SCL, SDA Output	VOL	0		0.4	V	
	VOH	Vcc-0.5		Vcc+0.3	V	
ESD Specifications						
Electro-Static Discharge	Human Body Model (HBM, MIL_STD 883 Method 3015.7)			1000	V	high speed pins
Electro-Static Discharge				2000	V	all other pins

High Speed Electrical Specifications

Parameter	Min	Typ	Max	Units
Module Electrical Input Characteristics				
Signaling rate per lane ± 100 ppm		26.5625		GBd
Differential peak-to-peak input voltage tolerance	900			mV
Differential termination mismatch			10	%
Single-ended voltage tolerance range	-0.4		3.3	V
DC common mode voltage	-350		2850	mV
Module Electrical Output Characteristics				
Signaling rate per lane ± 100 ppm		26.5625		GBd
AC common-mode output voltage RMS			17.5	mV
Differential peak-to-peak output voltage			900	mV
Near-end eye symmetry mask width (ESMW)		0.265		ui
Near-end eye height, differential	70			mV
Far-end eye symmetry mask width (ESMW)		0.2		ui
Far-end eye height, differential	30			mV
Far-end pre-cursor ISI ratio	-4.5		2.5	%
Differential termination mismatch			10	%
Transition time, 20-80%	9.5			ps
DC common mode voltage	-350		2850	mV

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
PAM4 Signaling rate, each lane (±100ppm)	Boptic		53.125		GBd	
Lane Wavelength	λ0	1304.5		1317.5	nm	
Side-mode Suppression ratio	SMSR	30			dB	
Average Launch Power	PAVG	-2.9		4.0	dBm	1
Optical Modulation Amplitude (OMAouter)	POMA	-0.8		4.2	dBm	
Launch Power in OMA minus TDECQ		-2.2			dB	
Transmitter and Dispersion Eye Closure for PAM4, each lane	TDECQ			3.4	dB	2
Average Launch Power OFF Transmitter, each lane	Poff			-15	dBm	
Extinction Ratio, each lane	ER	3.5			dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance	RL			-26	dB	
RIN21.4 OMA				-136	dB/Hz	
Receiver						
PAM4 Signaling rate, each lane (±100ppm)	Boptic		53.125		GBd	
Lane Wavelength	λ0	1304.5		1317.5	nm	
Damage Threshold	THd	5			dBm	3
Average Receive power	ROP	-5.9		4	dBm	4
Receiver Power (OMAouter)				4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter)				-4.4	dBm	
Stressed Receiver Sensitivity (OMAouter)	SRSmask			-1.9	dBm	5
Stressed Conditions for Stress Receiver Sensitivity						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	0.9		3.4	dB	
OMAouter of each aggressor lane				4.2	dBm	
Rx_LOS Assert Level	LOSA	-16			dBm	
Rx_LOS De-Assert Level	LOSD			-7.5	dBm	
Rx_LOS Hysteresis	LOSHys	0.5			dB	

Notes:

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level.
4. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

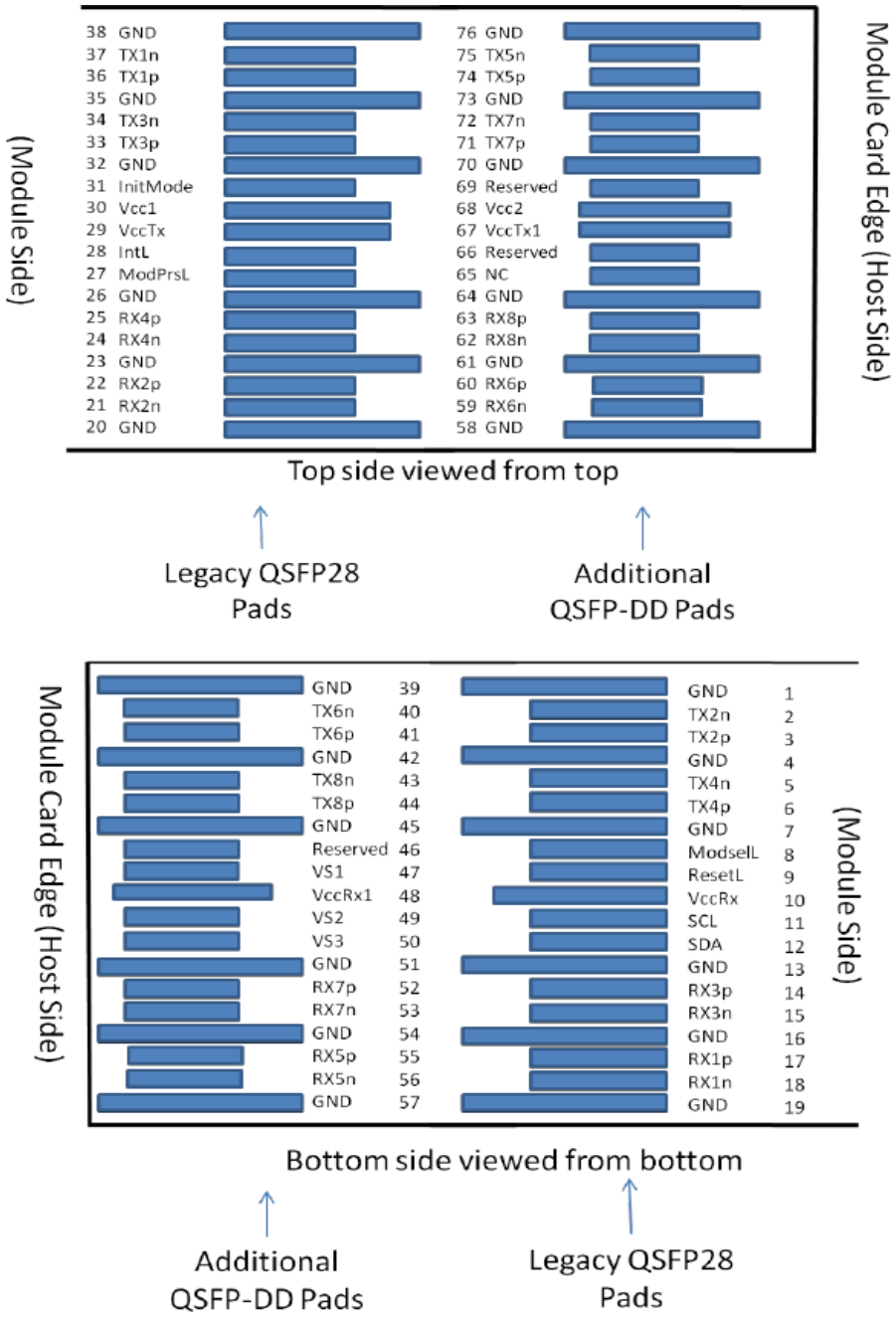
5. Measured with conformance test signal at TP3 for BER = 2.4x10-4. A compliant receiver shall have stressed receiver sensitivity (OMA outer), each lane values below the mask, for SECQ values between 0.9 and 3.4 dB.

Pin Descriptions

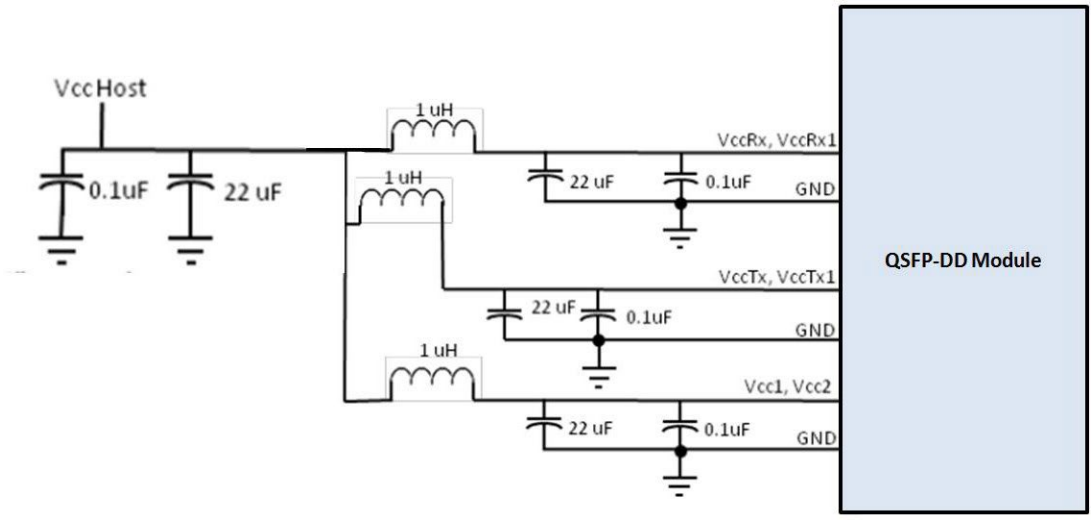
Pin	Logic	Symbol	Name/Descriptions	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B

35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
67		GND	Ground	1A
68		NC	No Connect	3A
69		Reserved	For future use	3A
70		VccTx1	3.3V Power Supply	2A
71		Vcc2	3.3V Power Supply	2A
72		Reserved	For Future Use	3A
73		GND	Ground	1A
74	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx7n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

QSFPDD Connector Pin Definition



Recommended Power Supply Filter

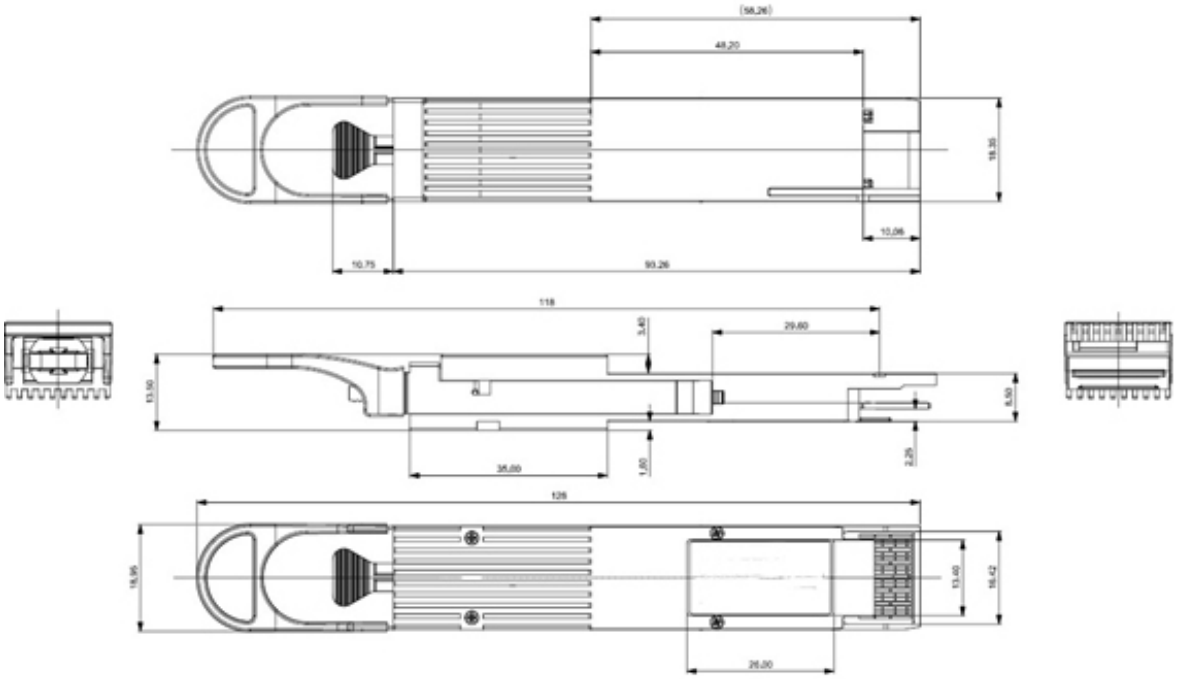


Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Accuracy
Module Monitor 1: Temperature	± 3 C
Module Monitor 2: Supply 3.3 voltage	± 0.1 V
Lane Monitor: TX output optical power	± 3 dB
Lane Monitor: TX bias current	± 10 %
Lane Monitor: RX input optical power	± 3 dB

Mechanical Specifications



About Us:

Proline Options is one of North America's leading providers of transceivers and high speed cabling. With a reputation for quality, tested products that cover the connectivity spectrum, Proline Options has a solution for you regardless of the specification.

At Proline Options, every product is tested in its intended application - never batch or spec tested only. We run bandwidth, distance and IOS network tests. We have documented an impressive 0.03% failure rate over the last 10 years. To continue this rate of success we invest millions annually in our own on-site testing lab.

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